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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,254	06/26/2003	Talal K. Jaber	42P15218	7766

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,254	JABER ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☒ Claim(s) *25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a Non-Final Office Action in response to the present U.S. Application filed 6/26/2003. Claims 1-31 are pending and presently under examination.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "audio device" recited in claim 18 must be shown or the feature canceled from the claims. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

Claim 25 is objected to because of a grammatical error: On line, "operated" should be changed to "operate". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Jaber (U.S. Patent No. 6,028,983), issued: February 22, 2000.

Regarding independent Claim 1, Jaber discloses an apparatus for testing a microprocessor chip 12, using dedicated scan strings, see Figures 1-7, comprising:

First and second control means compatible (JTAG port 22, Figures 1 and 5), which receives, at clock unit 39, TCK system and TMS master scan clocks corresponding to functional and scan clock, respectively. The (clock unit 39) routes scan clock signals C1/C2 to the scan clock generate logic unit 49, which generates a set of clock signals including a master functional clock signal, a slave functional clock signal, a master scan clock (A) signal and a slave scan clock (B) signal, and where the unit 49 provides the set of clock signals to flip-flops or latches in each functional unit (26 thru 40), within the integrated circuit (microprocessor chip 12). It is noted that the first and second control means corresponding to (JTAG port 22, Figures 1 and 5) be functionally independent of each other, since unit 49 generates independent functional and scan clocks in response to scan clock signals C1/C2, which may be at frequencies.

Regarding Claim 2, Jaber discloses second control means (compatible JTAG port 22, Figures 1 and 5) for receiving a scan train for verifying the logical design of the chip or performing a boundary scan test, comprising units (39, 47, 49, 51), which perform the equivalent functions corresponding to a cluster test controller, a unit test controller, and a local test clock controller coupled to each other in a logical hierarchy to control the functional unit independently of any other functional unit.

Regarding Claim 3, Jaber discloses functional units FUBs, such as processor functional units (26 . . . 41, see Figure 4), designated as: Instruction Fetch Unit (IFU) 26; Bus Interchange Unit (BIU) 28; Floating Point Unit (FPU) 30; File Exchange Unit (FXU) 32; Load and Store Unit (LD/ST) 34; Direct Cache Unit (DCU) 36; Instruction Processing Unit (IPU) 38; and Memory Management Unit (MMU) 41, as shown in Figure 3.

Regarding Claims 4, 5, Jaber discloses a third clock means (scan clock generate logic unit 49) for partially controlling the plurality of FUBs functional units (26 . . . 41, see Figure 4), described in claim 3 above, wherein the third clock means 49 receives at frequencies C1/C2, from the clock unit 39, and together with inputs from the decoder 45 and options register generates a set of clock signals including a master functional clock signal; a slave functional clock signal; a master scan clock (A) signal and a slave scan clock (B) signal. The unit 49 provides the set of clock signals to flip-flops or latches (not shown) in each functional unit.

Regarding Claims 6, 7, Jaber discloses first and second control means compatible (JTAG port 22, Figures 1 and 5) to control the functional units (26 . . . 41,

see Figure 4), described in claim 3 above, during normal operation using (functional clock), and during testing using (scan clock), through multiplexer 47, which directs the scan train to selected functional units 26 thru 41 (Figure 4) according to the instructions received from the decoder 45 and the options register 44. Each microprocessor functional unit (26 thru 40) receives a dedicated portion of the scan train 25, shown in Figure 4 as (scan string 0, 1 . . .n) where "n" is the total number of units in the microprocessor 12.

Regarding independent Claim 8, Jaber discloses a microprocessor chip 12, comprising:

A functional clock hierarchy and a scan clock hierarchy as shown in Figure 4, in a compatible (JTAG port 22, Figure 1), which is a representation of dedicated scan sub-units (40.sup.1. . . 40.sup.12), each scan sub-unit is dedicated to a particular functional unit (26 . . . 41, see Figure 4), for operation of functional units of microprocessor 12, at a at a first set of clock speeds and at a second set of clock speeds corresponding to master and slave functional clocks having a first speed corresponding to clock frequency (C1), and having a second speed corresponding to clock frequency (C2), where the clock signals C1 and C2 are at different frequencies, and therefore C1 may be slower than C2 and vise versa.

Regarding Claims 9-14, Jaber discloses compatible JTAG port 22, Figures 1 and 4, for receiving a scan train for verifying the logical design of the chip or performing a boundary scan test, comprising units (39, 47, 49, 51), which perform the equivalent

functions corresponding to the claimed features of a cluster test controller, a unit test controller, and a local test clock controller coupled to each other in a logical hierarchy to control the functional unit independently of any other functional unit.

Regarding Claim 15, Jaber discloses (scan clock generate logic unit 49) for testing FUBs functional units (26 . . . 41, see Figure 4), using the generated set of clock signals including a master functional clock signal; a slave functional clock signal; a master scan clock (A) signal and a slave scan clock (B) signal. The unit 49 provides the set of clock signals to flip-flops or latches (not shown) in each functional unit, for testing the functional units.

Regarding Claim 16, Jaber discloses an instruction register 43, which provides instructions through decoder 45 to a multiplexer 47 for selecting a first and a second set of functional units (26 . . . 41, Figure 4), and wherein the first and a second sets operating concurrently with the functional clock speed and the scan clock speed, using a first set of clocks corresponding to master and slave functional clocks having a functional clock speed at frequency (C1), and using a second set of clocks corresponding to master and slave scan clocks having a scan clock speed at frequency (C2), for operating the selected functional units (26 . . . 41, Figure 4), where clock frequency (C1) and clock frequency (C2), may have the same frequency, thus having the same speed, and therefore operating concurrently.

Regarding Claim 17, the scan clock hierarchy is to be used during testing of the microprocessor 12, using multiplexer 47, which directs the scan train to selected functional units 26 thru 41 (Figure 4). Each microprocessor functional unit 26 thru 41

receives a dedicated portion of the scan train 25, shown in Figure 4 as (scan string 0, 1 . . .n) where "n" is the total number of units in the microprocessor 12.

Regarding independent Claim 18, Jaber discloses in Figure 1, a test system 10, comprising:

A memory unit (permanent storage 13) coupled to microprocessor 12 through a cable 14; connector 16; buffer 18 and a JTAG bus 20, and wherein an audio device is inherently part of the workstation 11. Each chip 12 includes a compatible JTAG port 22 for receiving a scan train for verifying the logical design of the chip or performing a boundary scan test. The test system includes a workstation 11 capable of running large programs from the permanent storage 13.

The microprocessor 12 comprising a functional clock hierarchy and a scan clock hierarchy as shown in Figure 4, in a compatible (JTAG port 22, Figure 1), which is a representation of dedicated scan sub-units (40.sup.1. . . 40.sup.12), each scan sub-unit is dedicated to a particular functional unit (26 . . . 41, see Figure 4), for operation of functional units of microprocessor 12, at a at a first set of clock speeds and at a second set of clock speeds corresponding to master and slave functional clocks having a first speed corresponding to clock frequency (C1), and having a second speed corresponding to clock frequency (C2), where the clock signals C1 and C2 are at different frequencies, and therefore C1 may be slower than C2 and vise versa.

Regarding Claim 19, Jaber discloses an instruction register 43, which provides instructions through decoder 45 to a multiplexer 47 for selecting a first and a second set

of functional units (26 . . . 41, Figure 4), and wherein the first and a second sets operating concurrently with the functional clock speed and the scan clock speed, using a first set of clocks corresponding to master and slave functional clocks having a functional clock speed at frequency (C1), and using a second set of clocks corresponding to master and slave scan clocks having a scan clock speed at frequency (C2), for operating the selected functional units (26 . . . 41, Figure 4), where clock frequency (C1) and clock frequency (C2), may have the same frequency, thus having the same speed, and therefore operating concurrently.

Regarding Claim 20, 22, a scan train 40 (n), relating to automatic test pattern string, is supplied to the terminal TDI and serially passed through each of the functional units of the chip 12 unit for functional or scan test (Figures 4, 5 and 6)

Regarding Claim 21, Jaber discloses a microprocessor chip 12 comprising (JTAG port 22, Figures 1 and 5), which receives TCK system and TMS master scan clocks corresponding to functional and scan clock, respectively, independently of each other, and generate, using logic unit 49, a master functional clock signal, a slave functional clock signal, a master scan clock (A) signal and a slave scan clock (B) signal, to drive the functional and scan clock chains independently, Figure 6.

Regarding Claim 23, Jaber discloses a plurality of outputs (TD) of the master latches and slave latches are supplied to the scan train, which after passing through all of the functional units is returned to the test processor through the terminal TDO. The test result derived from the scan string for a particular functional unit is returned to the multiplexer 53, and provided to the output terminal TDO, Figures 4 and 6.

Regarding Claim 24, Jaber discloses plurality of inputs (DTI) and a plurality of outputs (TDO), which may vary in number depending on the test I/O requirement for each microprocessor chip 12 under test, Figure 4.

Regarding Claim 25, a functional clock hierarchy and a scan clock hierarchy as shown in Figure 4, in a compatible (JTAG port 22, Figure 1), which is a representation of dedicated scan sub-units (40.sup.1 . . . 40.sup.12), each scan sub-unit is dedicated to a particular functional unit (26 . . . 41, see Figure 4), for operation of functional units of microprocessor 12, at a at a first set of clock speeds and at a second set of clock speeds corresponding to master and slave functional clocks having a first speed corresponding to clock frequency (C1), and having a second speed corresponding to clock frequency (C2), where the clock signals C1 and C2 are at different frequencies, and therefore C1 may be slower than C2 and vise versa.

Regarding independent Claim 26, Jaber discloses an apparatus for testing a microprocessor chip 12, comprising:

a functional clock hierarchy and a scan clock hierarchy as shown in Figure 4, in a compatible (JTAG port 22, Figure 1), which is a representation of dedicated scan sub-units (40.sup.1 . . . 40.sup.12), each scan sub-unit is dedicated to a particular functional unit (26 . . . 41, see Figure 4), for operation of functional units of microprocessor 12, at a at a first set of clock speeds and at a second set of clock speeds corresponding to master and slave functional clocks having a first speed corresponding to clock frequency (C1), and having a second speed corresponding to clock frequency (C2),

where the clock signals C1 and C2 are at different frequencies, and therefore C1 may be slower than C2 and vise versa.

Furthermore, Jaber discloses compatible (JTAG port 22, Figures 1 and 5) for receiving a scan train for verifying the logical design of the chip or performing a boundary scan test, comprising units (39, 47, 49, 51), which perform the equivalent functions corresponding to a cluster test controller, a unit test controller, and a local test clock controller coupled to each other in a logical hierarchy to control the functional unit independently of any other functional unit.

Regarding Claims 27-30, Jaber discloses compatible JTAG port 22, Figures 1 and 4, for receiving a scan train for verifying the logical design of the chip or performing a boundary scan test, comprising units (39, 47, 49, 51), which perform the equivalent functions corresponding to the claimed features of a cluster test controller, a unit test controller, and a local test clock controller coupled to each other in a logical hierarchy to control the functional unit independently of any other functional unit.

Regarding Claim 31, Jaber discloses (scan clock generate logic unit 49) for testing FUBs functional units (26 . . . 41, see Figure 4), using the generated set of clock signals including a master functional clock signal; a slave functional clock signal; a master scan clock (A) signal and a slave scan clock (B) signal. The unit 49 provides the set of clock signals to flip-flops or latches (not shown) in each functional unit, for testing the functional units.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2133

By: _____

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